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| 09/630,883 | 08/02/2000 | Khosrow Golshan | 82259/156 | 7954 |

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|---|---|
| CHANG, AUDREY Y | |
| ART UNIT | PAPER NUMBER |
| 2872 | |

DATE MAILED: 12/03/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/630,883 | Applicant(s) GOLSHAN, KHOSROW | |
|---|---|---|---|
| | Examiner Audrey Y. Chang | Art Unit 2872 | |

*-- Th MAILING DATE of this communication appears n th cov r sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) *23-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 31-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election with traverse of invention group I of claims 1-22 and 31-46 in Paper No. 4 is acknowledged. The traversal is on the ground(s) that the non-elected claims 23-30 are drawn to "method for making optical logic gate" which therefore should not be restricted out from the elected claims that are drawn to "optical logic gate". This is not found persuasive because although the non-elected claims 23-30 claim a method for making "optical logic gate" however such limitation is only in the preamble and **no specifics** concerning the optical logic gate are recited in the claims. The claims rather are drawn to a method for laying several layers that could amount to anything not necessary to an optical logic gate. The claims in group I and group II are therefore **patentably distinct** from each other.

**The requirement is still deemed proper and is therefore made FINAL.**

2. Claims 23-30 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 4.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 1-10, 11-22, 31-35 and 36-46 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The interference effect, between the optical input signals, is critical or essential to the practice of the invention, but not included in the claim(s) (1, 11, 31, 36) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA**

1976). The specification fails to teach adequately as how could a Boolean logic output be provided by simply having a plurality of optical pathways in the optical layer and simply based on the optical output.

The specification also fails to disclose what does it mean by "optical bias" and fails to teach adequately as how to produce such "optical bias".

The specification also fails to disclose how could "at least two (or three) optical conduits configured to receive **an** optical input", as recited in claims 12 and 14. The specification only gives the support for one optical conduit to receive one optical input.

Claims 2-10, 12-22, 32-35 and 37-46 inherit the rejections from their respective based claim.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

**6. Claims 1-10, 11-22, 31-35, and 36-46 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

The phrases "optical input", "optical bias", "bias input" and the "optical output" recited in various claims appear to be vague and indefinite since it is not clear if they are referred to **physical structures** for relaying various light signals to the logical gate or they are referred to the actual **light signals** that propagated though the optical logical gate.

Claims 1, 11, 31 and 36 are rejected under 35 U.S.C. 112, second paragraph, as being **incomplete** for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the interference region or effect.

Claims 2-6, 12-13, 14-16, 32, and 37-41 are rejected under 35 U.S.C. 112, second paragraph, as being **incomplete** for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted

structural cooperative relationships are: among the optical pathways or optical conduits and the interference region and among the "optical input", the "first selective input", "an optical bias", "a bias input" "an interference region output", and "second selective input" recited in various claims. These lacking of the structural and logical relationships make the scopes of the claims unclear.

The phrase "the interference region includes a first selective input, a bias input and an interference region output" recited in claims 3 and 38 appears to be vague and indefinite since the interference region may be **coupled to** the input, output and bias input but it certainly does not include them.

The phrase "is representative of the NOT (or NOT AND (NAND)) function" appears to be confusing since it is not clear what does this "representative" mean. If the logic output function is a NOT or NAND function then specifically states so.

The phrase "having a plurality of optical logic gates configured to function as an optical processor" recited in claims 9 and 44 appears to be vague and indefinite since it is not clear what are these "optical logical gates" referred here. It is also not clear how does these optical logical gates relate to the elements recited in its base claims (1 and 36). The phrase "is comprises" recited in claims 10 and 45 appears to be vague an indefinite. The scopes of the claims are therefore not clear.

The phrase "at least two of the optical inputs" recited in claim 16 appears to be vague and indefinite since it lacks proper antecedent basis from its based claim.

The phrase "providing a light" recited in claim 31 appears to be vague and indefinite since it is not clear how does this phrase relate to the phrase "providing light to the at least one optical input" recited in earlier part of the claim.

Claim 41 appears to be confusing, in error and indefinite in particular it is not clear what does the phrase "and light is provided to neither of the first and second selective inputs" mean. The scope of the claim therefore is unclear.

**Claims as stand now contain numerous errors, confusions, inconsistent terms and phrases, and indefiniteness.** The examiner can only point out a few. It is the **applicant's responsibilities** to clarify **ALL** of the discrepancies in the claims to make them in comply with the requirements of 35 USC 112. The dependent claims inherit the rejections from their various based claims.

***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**8. Claims 11, 16, 36-37, 43 and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by the patent issued to Utaka et al (PN. 5,315,422).**

Utaka et al teaches an *interference type optical logic element* for controlling optical signal by light, i.e. an *optical processor*, that is comprised of

(1) a *substrate* (3) of a *first semiconductor material*, and

(2) a *patterned optical layer* (7) overlaying the substrate of a *second semiconductor material.*

Utaka et al teaches that the optical layer (7) is patterned with a plurality of *optical waveguides* serve as the *optical conduits* (I and II) with at least one of the optical conduits receives an optical input light signal ($P_i$) and at least one of the optical conduits configured to provide an optical output light signal ($P_o$), (please see Figures 2A, 2B, 3-5, 6A and 7-10). The input light signal propagates through the plurality of the waveguides or conduits to reach a region such that the light signals from the various waveguides interfere to each other wherein the interference causes the output light signal to perform a Boolean logical function, (please see columns 4-5).

With regard to claims 43 and 46, Utaka et al teaches that the optical logic element may perform logic functions such as NAND and XOR, (please see column 8).

This reference has therefore anticipated the claims.

**9. Claims 31-33 are rejected under 35 U.S.C. 102(b) as being anticipated by the patent issued to Yang (PN. 5,239,173).**

Yang teaches a binary data processor for providing various logical functions wherein the processor comprises a coherent light source (11) for *providing light* through *light pipes* (41) serve as *the plurality optical pathways* and *slits* (13 and 14) serves as the *optical inputs* to a portion such that the light from the plurality of pathways or light pipes interfere with each other, (please see Figures 4 and 5, column 4). The interference pattern is transmitted via output light pipes (42) or fiber optic bundle (43) as the optical output light signal that may represent various logic functions such as AND, OR and NOT. This reference has therefore anticipated the claims.

***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**11. Claims 12-15 and 17-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Utaka et al.**

The interference type optical logic element taught by Utaka et al as described for claim 11 above has met all the limitations of the claims.

With regard to claims 12-15, Utaka et al teaches that the patterned optical layer may have two or three waveguides or conduits for receiving optical input light signal to perform various logical operations such as AND, NAND, OR, XOR, NXOR. However this reference does not teach explicitly that the input light signals are biased and the logical function is NOT. But since the specification of the instant application fails to teach what is considered here to be an "optical bias" such feature therefore cannot be addressed. Although this reference does not teach explicitly to have the NOT logic function however since this is one of the most standard logic functions in the art. Incidentally, both NAND and NXOR functions include NOT function. And since this reference teaches explicitly to induce phase difference among the optical input light signals to create the various logic functions to modify the logic element to perform the NOT logic function would have been obvious to one skilled in the art since it has been held when the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With regard to claims 17-20, Utaka et al teaches that the optical layer or the substrate may be formed by doped Gallium Arsenide, (please see column 1). However it does not teach explicitly that it may also be formed by doped silicon. However doped silicon is a very well known semiconductor material for making logic circuit in the art and since the specification fails to teach the criticality of having this particular material would overcome any problem in the prior art such modification would have been obvious matter design choice to one skilled in the art.

With regard to claims 21 and 22, Utaka et al teaches that a semiconductor DFB laser may be used as the light source to provide the input light signals, (please see Figure 8A and column 8).

**12. Claims 34 and 35 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over the patent issued to Yang.**

The optical binary data processor that performs logical functions taught by Yang as described for claim 31 above has met all the limitations of the claims. Yang further teaches that logic circuit system having multiple logic steps can be constructed from combination of basic logic functions AND, OR and NOT. In Figure 6, Yang teaches a data processor system having a cascaded series of N optical processing steps that may include various combinations of the basic logic functions. Although this reference does not teach explicitly to have NOT AND (NAND) function and to have NOT and NOT AND function however since these functions are combinations of the basic logic functions they are therefore either implicitly included or obvious modifications to one skilled in the art.

13. **Claims 1-10, 38-42, and 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Utaka et al.**

Utaka et al teaches an *interference type optical logic element* for controlling optical signal by light, i.e. an *optical processor*, that is comprised of

(1) a *substrate* (3) of a *first semiconductor material*, and

(2) a *patterned optical layer* (7) overlaying the substrate of a *second semiconductor material.*

Utaka et al teaches that the optical layer (7) is patterned with a plurality of *optical waveguides* serve as the *optical pathways* (I and II) with at least one of the optical pathways receives an optical input light signal ($P_i$) and at least one of the optical pathways configured to provide an optical output light signal ($P_o$), (please see Figures 2A, 2B, 3-5, 6A and 7-10). The input light signal propagates through the plurality of the waveguides or pathways to reach a region such that the light signals from the various waveguides interfere to each other wherein the interference causes the output light signal to perform a Boolean logical function, (please see columns 4-5).

This reference has met all the limitation of the claims with the exception that is does not teach explicitly that at least one of the optical pathway transmits a biased optical signal. However since the specification of the instant application fails to teach what is considered to be an "optical bias" such feature therefore cannot be addressed here.

With regard to claims 3-8 and 38-42 Utaka et al teaches that the patterned optical layer may have two or three waveguides or pathways for receiving optical input light signal to perform various logical operations including AND, NAND, OR, XOR, NXOR. Although this reference does not teach explicitly to have the NOT logic function however since this is one of the most standard logic functions in the art. Incidentally, both NAND and NXOR functions include NOT function. And since this reference teaches explicitly to induce phase difference among the optical input light signals to create the various logic functions to modify the logic element to perform the NOT logic function would therefore have been obvious to one skilled in the art since it has been held when the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With regard to claims 9-10 and 44-45, Utaka et al teaches that the optical logic element is used as optical processor for processing and controlling optical signals. Utaka et al also teaches that a plurality of optical logic elements may be integrated such that a combination of basic logic functions (AND, OR and NOT) can be achieved to provide more complicated logic function such as NAND, XOR and NXOR. Although this reference does not teach explicitly to have the combined NOT and NAND functions such modification would have been obvious to one skilled in the art since it simply involves combining these elements for the purpose of performing the desired logic function.

***Double Patenting***

14. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ...

may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

15. Applicant is advised that should claims 11 and 16 be found allowable, claims 36-37 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Audrey Y. Chang whose telephone number is 703-305-6208. The examiner can normally be reached on Monday-Friday (8:00-4:30), alternative Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Cassandra Spyrou can be reached on 703-308-1637. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

*Audrey Y. Chang*
*Primary Examiner*
*Art Unit 2872*

A. Chang, Ph.D.
November 21, 2001